REMARKS

Claims 1-5, 10-12 and 15-20 are pending in the present application after entry of the present amendment. Claims 1-5 were rejected under 35 U.S.C. 112. Claim 10 is rejected under 35 U.S.C. 102. Claims 1-5, 10-12, 15-16, and 17-20 were rejected under 35 U.S.C. 103. The Applicant respectfully traverses the pending rejections.

Claim Rejections under 35 USC 112

Applicant has amended claim 1 per the Examiner's suggestion and to further clarify the input and output stages of the flip-flop. The Applicant requests this rejection be withdrawn.

As claims 2-5 were rejected to as being indefinite because claim 1 was rejected to as being indefinite, Applicant requests that in light of amended claim 1, the rejection to claims 2-5 be withdrawn.

Claim Rejections under 35 USC 102

Claim 10 was rejected under 35 U.S.C. 102(b) as being anticipated by Timoc (U.S. Patent No. 6,002,270). Paragraph 6 of the Office Action mailed February 27, 2004 was unclear on which claim was rejected 15, 1, or 10. In a phone interview with Examiner Nguyen on April 22, 2004 (as memorialized by an Interview Summary mailed April 28, 2004), it was agreed that claim 10 was rejected.

Claim 10 has been amended to recite, among other features: a cross coupled circuit having a cross coupled transistor directly connected to a positive power supply voltage, wherein a gate of the cross coupled transistor is connected to the second output terminal. FIG. 5 of Timoc neither discloses nor suggests such a cross coupled circuit. Hence, this rejection should be withdrawn and claim 1 should be allowable.

Rejections under 35 U.S.C. 103

Claim 1 was rejected under 35 U.S.C. 103 as being unpatentable over Furuki (U.S. Patent No. 5,384,493) in view of Choe (U.S. Patent No. 6,373,292). In Figure 2 of Choe, there is a transistor, e.g., 58, between the output terminals 58 and 60 which is turned on and off by a clock. In Figure 13 of Furuki a D flip-flop having a cascade of two circuits 20b and 20c is shown. When the clock signal CLKb is of a high level, the circuit 20b delivers its output signals to the output terminals OUT1 and OUT2 based upon the input signals D and Db. At this time, the circuit 20c keeps output levels on its output terminals OUT3(Q) and OUT4(Qb) irrespective of the levels of the output signals on the output terminals OUT1 and OUT2 of the circuit 20c. Once the clock signal CLK is at a high level, the circuit 20c delivers its outputs onto the output terminals OUT3(Q) and OUT4(Qb) in conformity with the output levels in the output terminals OUT1 and OUT2 of the circuit 20b, thereupon, the circuit 20b keeps its output levels dependent upon the levels of the input signals D and Db before the clock signals CLKs change to the high level. Accordingly, when the clock signal CLK is of the high level (CLKb at low level), the output levels on the output terminals OUT3(Q) and OUT4(Qb) are kept unchanged even if the levels of the input signals D and Db change (col. 10, lines 13-30).

With respect to claim 1, combining Choe with Furuki as the Office Action suggests would change the principle of operation of the circuit of Fig. 13 of Furuki, and thus cannot be used to establish a prima facie case of obviousness. The modification to FIG. 13 proposed by the Office Action is a first transistor connected between nodes OUT1 and OUT2 of circuit 20b with a gate connected to CLK and a second transistor connected between nodes OUT3 and OUT4 of circuit 20c with a gate connected to CLKb. In this modified circuit 20b, when CLKb is high, the modified circuit 20b delivers its output signals to the output terminals OUT1 and OUT2 based upon the input signals D and Db. When CLK the goes high (CLKb goes low), OUT1 and OUT2 are shorted

together via the first transistor, and since transistors Q67 and Q68 are also turned on as CLK is high, OUT3 is equal to OUT4 and not Q and Qb (e.g., rather than Q=1 and Qb=0 (or Q=0 and Qb=1), Q=Qb=some intermediate value). Thus the circuit in FIG. 13 no longer works as a D flip-flop. As the modification to FIG. 13 of Furuki suggested by the Office Action changes the principle of operation of Furuki, the rejection should be withdrawn and claim 1 should be allowable.

Claims 2-5 which depend upon claim 1 should be allowable for at least the same reason claim 1 is allowable.

Claim 10 was rejected under 35 U.S.C. 103 as being unpatentable over Hwang et. al. (U.S. Patent No. 5,777,491) in view of Timoc. The Office Action combined the transistor 11 in Figure 5 of Timoc with Figure 1 of Hwang, by connecting the transistor 11 between nodes Q and QN of Figure 1 of Hwang.

The Office Action's proposed modification changes the principle operation of Hwang and thus cannot be used to establish a prima facie case of obviousness. First, Figure 1 of Hwang has no clock, it is an asynchronous circuit. Next, regardless of what the input is, either circuit 11 is pulled to ground (A=B=1) and node Q is pulled high (circuit 12 is off) or circuit 12 is pulled to ground (A=0 or B=0) and node QN is pulled high (circuit 11 is off). Adding the transistor 11 between nodes Q and Qn would periodically (when CLK=1) try to set Q=QN. Thus the combinational logic circuit of Hwang (Q=AB and QN=AN+BN, col. 2, lines 17-18), which outputs a 1 or 0, is now modified to output a 1 or 0 with periodic outputs of uncertainty (depending on the state of a clock, i.e., a synchronous circuit). As the modification to FIG. 1 of Hwang suggested by the Office Action changes the principle of operation of Hwang, the rejection should be withdrawn and claim 10 should be allowable.

Claims 11, 12, 15, and 16, which ultimately depend upon claim 10, should be allowable for at least the same reason claim 10 is allowable.

Claim 17 was rejected under 35 U.S.C. 103 as being unpatentable over Furuki in view of Choe, as discussed in claim 1 and in further view of Tung (U.S. Publication No. 2003/0052720 A1).

For at least the above reasons given for claim 1, claim 17 should be allowable.

Claims 18-20 which ultimately depend upon claim 17 should be allowable for at least the same reasons claim 17 is allowable.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicant's attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on May 20, 2004.

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